REMARKS

Claims 1 - 4 and 6 - 16 remain active in this application. Claim 5 has previously been canceled. An editorial revision otherwise done throughout the claims in the previous response has been requested in claim 1. No other amendments are presented herein and no new matter has been introduced into the application.

The indication of allowability of claims 3 - 4 and 13 - 15 subject to being rewritten in independent form is noted with appreciation. The Examiner has objected to these claims as depending from rejected claims. However, since the grounds of rejection asserted in regard to other claims are believed to be improper as will be discussed in detail below, Applicant respectfully declines to rewrite these claims in independent form at this time.

Claims 6 - 10 have been rejected under 35 U.S.C. §102 as being anticipated by the newly cited Johnson publication and claims 1, 2, 11 - 12 and 16 have been rejected under 35 U.S.C. §103 as being unpatentable over Hunt in view of Johnson. These grounds of rejection are both respectfully traversed.

In regard to the rejection of claims 6 - 10 for anticipation by Johnson, it is respectfully submitted that the Examiner's explicitly stated rationale for the rejection of these claims provides ample evidence of the impropriety thereof. Specifically, the Examiner merely asserts that "pages 44 - 49 of Johnson predate applicant's filing by almost a decade" and " [t]hey teach the *concepts* being claimed in claims 6 - 10 were old and well-known at the time of applicants filing" (emphasis added). It is well-established that for anticipation to be demonstrated, each *element* or *step* being claimed must

be taught in a single reference. Therefore, it is respectfully submitted that demonstration that a *concept* is well-known is irrelevant to a demonstration of the *prima facie* propriety of an asserted ground of rejection. Moreover, the need to teach *claimed elements or steps* rather than *concepts* is not lessened by the period of time a reference purportedly teaching such concepts antedates the invention. Asserting or placing reliance on such period of time, as the Examiner has done, in effect, asserts (and assumes) that in such a period of time, someone is likely to have gained knowledge of the claimed subject matter (the fallacy in such a rationale being evident from the fact that problems encountered in many technologies have long remained unsolved, giving rise to the acceptance of evidence of "long-felt need" as secondary evidence of patentability) but does not provide actual *evidence* thereof which might support the asserted ground of rejection; which omission the assertion (or assumption) does not excuse. Rather, such a statement both admits and emphasizes that *evidence* necessary to support the asserted ground of rejection is not, in fact, provided by the reference relied upon. It is also respectfully submitted that such a position as has been taken by the Examiner is logically very similar to an "obvious to try" rationale under 35 U.S.C. §103 which has long been well-established to be " an unacceptable basis for rejection" as noted in, for example, In re David H. Fine, 5 USPQ 2d 1596 (Fed. Circ., 1988), citing, *inter alia*, In re Goodwin, 198 USPQ 1 (CCPA, 1978) but is clearly even more improper when such rationale is applied under 35 U.S.C. §102, as the Examiner has done here.

Substantively, it is also respectfully submitted that while Johnson, as understood from the pages relied upon and furnished with the current office action, may

teach issuance of instructions from both "in order" and "out-of-order" buffers (whether or not concurrently or simultaneously which does not appear particularly clear from the pages of Johnson relied upon and furnished with the current action) and the use of tags to indicate an uncomputed destination register (as contrasted with a tag bit to indicate whether or not a dependency exists or if the dependency exists, it remains uncanceled), Johnson teaches a very different constitution and operation of a reorder buffer than is provided in accordance with the present invention.

The invention provides a reorder buffer in which a queue control can be implemented which, in effect, provides additional order among the instructions which can *potentially* be issued out-of-order and, by doing so, achieves execution of a given set of operations in a reduced number of processing cycles as is well-illustrated in the comparison provided by and between Figures 8 - 11 and 12 - 14, respectively. That is, when the queue control is not exercised, the exemplary set of operations requires ten processing cycles whereas the same set of operations can be completed in nine processing cycles when the queue control, in accordance with the invention and providing that instructions are issued in order of storage entry number among instructions which have no uncanceled dependencies, is exercised. Also as well-illustrated in those respective Figures and described on pages 19 and 23, respectively, the invention allows earlier release of entries in the reorder buffer which improves processing efficiency and reduction of reorder buffer hardware requirements.

In sharp contrast therewith, Johnson teaches a reorder buffer constituted by a content-addressable memory notwithstanding the fact that such constitution

and operation necessarily allows ambiguous data in that the same register number may be "written into different entries in the reorder buffer" and which would all be returned when the reorder buffer is addressed by that content. The "correct value" is then found in Johnson by the buffer prioritizing the multiple matching entries by order of allocation and "returns the *most recent* entry" (emphasis added) to allow "new entries [to] supercede older entries"; *directly contrary to the claimed ordering of instruction issuance provided by the present invention*.

Perhaps even more importantly, while Johnson indicates that the superceded values may be discarded and removed from the associative lookup process, Johnson explicitly teaches that it is preferable *to preserve these values in the reorder buffer* to allow "the processor to recover the state associated with in-order completion, enabling the processor to implement precise interrupts." Such a retention of old values in a reorder buffer appears to be well-described as *an effect that the present invention avoids* (see page 2, line 5 - 14 of the original specification describing issuance of instructions without dependencies to the near-exclusion of instructions with dependencies which then accumulate in the reorder buffer and also requires greater hardware capacity for the reorder buffer which slows overall execution) and without discarding of any reorder buffer entries. Thus, Johnson teaches directly away from achievement of the meritorious effects of the invention while acknowledging a problem with the very different constitution and operation of the reorder buffer of Johnson and for which Johnson provides no solution due to a need for state recovery by reconstructing operations performed *without out-of-order issuance of instructions*.

From the forgoing, it is apparent the asserted rejection for anticipation by Johnson is clearly in error both by the Examiner's effective admission in the explicitly stated rationale for the rejection and substantively since Johnson fails to teach (or suggest) operations which answer the claim recitations but teach directly away therefrom; both in regard to the use of tags and the constitution and operation of a reorder buffer and also since those operations which substantively do not answer numerous claim recitations and are directly contrary thereto in the manner in which the reorder buffer prioritizes entries therein and other claimed features of the invention as discussed above in a manner quite similar to that presented in In re Fine, *supra*. Therefore, Johnson clearly fails to anticipate any of claims 6 - 10 and reconsideration and withdrawal of the asserted ground of rejection under 35 U.S.C. §102 is respectfully submitted to be in order.

By the same token, as discussed above, Johnson fails to provide an expectation of success in achieving the meritorious effects of the invention and, further, it appears that the approach taken by Johnson to constitution and operation of the reorder buffer may be even more subject thereto than more current known approaches while Johnson teaches that it is preferable to avoid the meritorious effects of reducing reorder buffer content (and capacity requirements) in order to be able to recover the processor state as if no reorder buffer had been provided or used. Therefore, the combination of Johnson with Hunt cannot mitigate the now admitted deficiencies of Hunt (or even be properly combined therewith under 35 U.S.C. §103) in regard to the subject matter of claims 1, 2, 11, 12 and 16, since Johnson teaches directly away from even the slightest vestige of

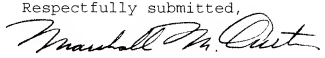
the meritorious effects of the invention and thus the combination of Hunt and Johnson cannot lead to an expectation of success in achieving those meritorious effect and thus cannot provide evidence of a level of ordinary skill in the art which would support the conclusion of obviousness which the Examiner has asserted. Accordingly, it is respectfully submitted that reconsideration and withdrawal of the asserted ground of rejection under 35 U.S.C. §103 is also in order and such action is respectfully requested.

It is also respectfully submitted that entry of the above-requested amendment is well-justified since it is limited to a minor editorial revision effecting only an improvement of form and which is not substantive. Further, the amendment merely completes a change otherwise carried out throughout the claims in the previous response. Therefore, no new issue can possibly be presented by the above-requested amendment. Moreover, the above-requested amendment clearly places the application in condition for allowance in view of the clear impropriety of the grounds of rejection as discussed above or, in the alternative, better form for Appeal by reducing potential issues. Accordingly, entry of the above amendment is respectfully requested.

Since all rejections, objections and requirements contained in the outstanding official action have been fully answered and shown to be in error, it is respectfully submitted that reconsideration is now in order under the provisions of 37 C.F.R. §1.111(b) and such reconsideration is respectfully requested. Upon reconsideration, it is also respectfully submitted that this application is in condition for allowance and such action is therefore respectfully requested.

If an extension of time is required for this response to be considered as being timely filed, a conditional petition is hereby made for such extension of time. Please charge any deficiencies in fees and credit any overpayment of fees to Attorney's Deposit Account No. 50-2041.

Respectfully submitted,



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